Alert on LAN* ASIC

Networking Silicon

Datasheet

Product Features

- Full system management solution with environmental instrumentation
- SMB interface to host
- Multiple transmissions of all SOS packets
- Five External maskable SOS events
- Automatic heartbeat generation when system is powered-off
- Watchdog timer for detection of system hang
- Power plane signal detection for low power state status
- Clock synchronization and smooth transition logic
- 82558 B-step Fast Ethernet** controller compliance only

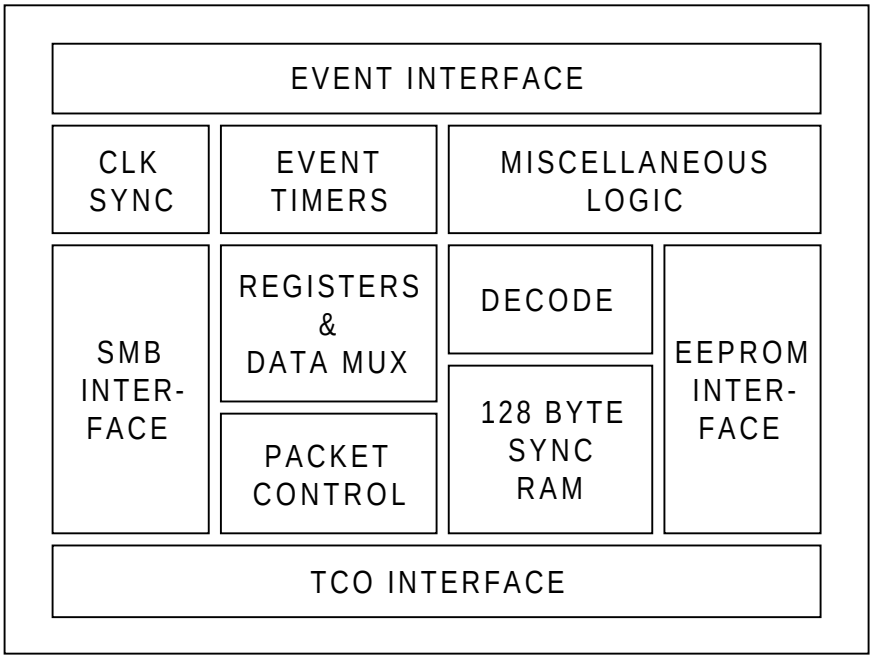

Figure 1. Alert on LAN ASIC Block Diagram

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Revision History

Revision Date	Version	Description
Oct. 1997	1.0	First release
Feb. 1998	1.1	General editing
July 1998	1.2	Expanded Section 2.4, "Event Interface" to include more detail and added Section 5.0, "Reset and Test Modes"

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1.0 Introduction

The Alert on LAN ASIC is intended to provide system manageability function to a desktop platform when used in conjunction with the Intel 82558 B-step (82558B) Fast Ethernet Controller. Together, these two integrated circuits (ICs) provide a management interface between a remote management console or server and the client system. Additional hardware is required to provide the Alert on LAN ASIC with system monitoring instrumentation (for example, over-voltage or over-temperature indications).

The Alert on LAN ASIC is not a stand alone device and requires the 82558B, a 64x16 EEPROM, environmental ICs, and support software to create a functional management solution. A more detailed description of the EEPROM and environmental ICs and other external components can be found in Section 8.0, “Appendix A: Alert on LAN Supporting Hardware” on page 31.

1.1 Alert on LAN Overview

The primary function of the Alert on LAN ASIC is to provide a transmit stream to the 82558B, which transmits alert (“SOS”) packets or heartbeat (“presence”) packets. The Alert on LAN ASIC is responsible for transmitting these packets when software is unable to (for example, during a low power state or system failure).

The Alert on LAN ASIC communicates to the system through a System Management Bus (SMB), which is a subset of the Phillips I^2C** interface. The SMB typically connects to the PCI-to-ISA/ IDE Xcelerator (PIIX4), which is accessible by the system and through the Basic Input/Output System (BIOS).

Communication between the Alert on LAN ASIC and the 82558B is through an 8-bit wide parallel data interface plus supporting control signals. The Alert on LAN ASIC uses this interface to transfer data for the transmission of packets, alert and heartbeat, to the 82558B.

The Alert on LAN ASIC transfers packets due to either internal or external events. External events are detected through five dedicated pins of the Alert on LAN ASIC; internal events are generated by either a set of timers or support software.

The Alert on LAN ASIC contains configuration registers to enable or disable events and store packet information. Since packets must be Internet Protocol (IP) routeable, the packet headers are stored in the Alert on LAN ASIC. The Alert on LAN ASIC does not have the resources necessary to create the correct IP packets and relies on supporting software and the IP stack to supply it with the appropriate information.

An external EEPROM is used to provide default configuration information to the Alert on LAN ASIC. It also provides the only method for loading a packet structure and header into the Alert on LAN ASIC. This allows the Alert on LAN ASIC to power-up into a configured state without the need for software configuration.

1.2 Management Overview

The Alert on LAN ASIC/82558B management solution is intended to provide system management capabilities including (but not limited to):

- SOS (alert) events
  - — Transmit SOS packets from preboot, the G0 State (working), the G1 State (sleeping), and the G2 State (soft-off)
  - — Transmit sender identification in SOS messages
    - – SOS hardware events
      - – Chassis intrusion
      - – Voltage out of specification
      - – Temperature out of specification
      - – LAN leash tamper
      - – Processor missing
    - – SOS software events
      - – OS lockup/system hang
      - – Failure to boot
      - – BIOS/System Management Interrupt (SMI) generated exception message
      - – Desktop Management Interface (DMI)/management agent generated exception message
- Presence heartbeat with status information

1.3 Alert on LAN Feature Set

The Alert on LAN ASIC includes the following features:

- Full system management solution with environmental instrumentation
- 82558 B-step controller compliance only
- SMB interface to host
- Multiple transmissions of all SOS packets
- Five external maskable SOS events
- Automatic heartbeat generation when system is in sleep or shutdown modes
- Watchdog timer for detecting system hang
- Power plane signal detection for low power state status
- Clock synchronization and smooth transition logic

1.4 Specifications and Standards Compliance

- Advanced Configuration and Power Interface Specification (ACPI), Revision 1.0
- Intel System Management Bus (SMB) Specification, Revision 1.0

2.0 Alert on LAN ASIC Architectural Overview

The internal architecture of the Alert on LAN ASIC is shown in Figure 1, “Alert on LAN ASIC Block Diagram” on the front cover.

2.1 TCO Interface

The TCO interface is a proprietary General Purpose Input/Output (GPIO) type of interface to the 82558B. It is an 8-bit parallel data interface along with several control signals. This interface is a unidirectional data bus. Data can only be transmitted from the Alert on LAN ASIC to the 82558B.

The TCO Read Request (TRDREQ) and TCO Active (TACTIVE) signals provide a handshaking mechanism that allows a GPIO type of interface.

The TCO Marker (TMARKER) pin is a signal that indicates whether the data on the bus is a command byte or a data byte. It is used to delineate datagrams on the TCO data bus.

The only command that the Alert on LAN ASIC uses on the TCO bus is the Transmit command. The format for the Transmit command on the TCO Marker (TMARKER) and TCO Data (TDATA[7:0]) lines to the 82558B is shown below.

TMARKER	TDATA[7:0] Bus
1	04h
0	FFh
0	00h
0	Data Byte 0
0	Data Byte 1
0	Data Byte 2
0	...
0	Data Byte N
1	00h

Additional signals are used to put the 82558B in or out of TCO mode.

The TCO Force (TFORCE) signal is an active high input that forces the 82558B into TCO mode. TFORCE is also used to end a TCO transaction. TFORCE will be forced inactive when any of the following conditions occur:

- Both the PCI Reset signal (PCI_RST#) and Main Power Good signal (PWR_GOOD) are active.
- The 82558 Software Reset (CTL_558RST) bit in the Control register is set (Section 4.11, “Register 9h; Control” on page 22).
- The Transmit Enable (CTL_TXEN) bit in the Control register is cleared (Section 4.11, “Register 9h; Control” on page 22).
- The TCO Ready Active (CTL_TRDY) bit in the Control register is set (Section 4.11, “Register 9h; Control” on page 22) and the TCO Ready (TREADY#) signal is inactive.

- The Alert on LAN Software Reset (TST_RST) bit in the Test Mode register is set (Section 4.15, “Register Dh; Test Mode” on page 23).

If a TCO transaction is aborted by any of the above mechanisms, except the TST_RST bit, the Alert on LAN ASIC will retry the transaction or start a new transaction with the prior status information when the condition that caused the abort no longer exists.

The TCO Status (TSTATUS#) signal is a pulse that indicates that the 82558B has completely processed the command. In the case of a Transmit command, this signal indicates that the packet has been sent on the wire or has been aborted due to transmission errors. This signal indicates to the Alert on LAN ASIC that the TFORCE signal should be de-asserted until the end of the TCO cycle.

The basic flow for a TCO cycle is:

1. The Alert on LAN ASIC samples the TACTIVE pin, which should be low prior to any TCO cycle. If it is sampled low, the ASIC asserts TFORCE to the 82558B.
2. The Alert on LAN ASIC asserts TRDREQ and transfers one byte (a command byte) and TMARKER to the 82558B at least two clock cycles after TFORCE was asserted.
3. The 82558B asserts TACTIVE upon completion of sampling the data.
4. The Alert on LAN ASIC samples TACTIVE high and de-asserts TRDREQ.
5. After the data is read by the 82558B and TRDREQ is de-asserted, the 82558B de-asserts TACTIVE.
6. The Alert on LAN ASIC repeats steps two through five for all bytes in a frame with TMARKER inactive for data bytes.
7. After the Alert on LAN ASIC has completed transferring a whole frame, it de-asserts the TFORCE pin.

The following diagram illustrates TCO timing for the Alert on LAN ASIC.

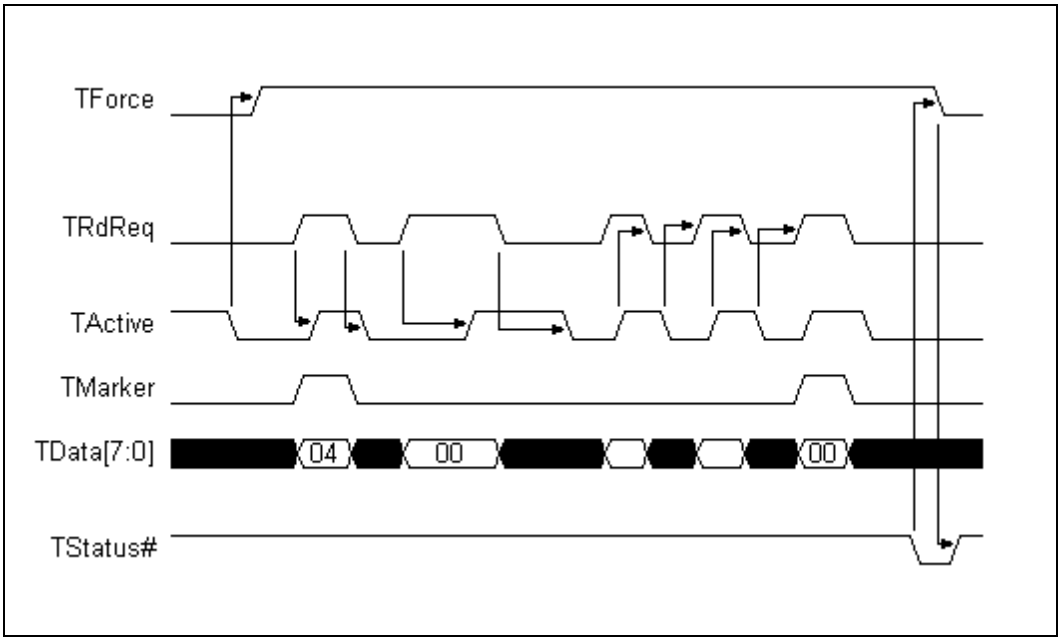

Figure 1. TCO Timing Diagram

2.2 SMB Interface

The SMB interface is a slave-only interface. Since the Alert on LAN ASIC is completely under software control and provides interrupts via the SMI output signal (SMI#), an SMB alert signal is not supported.

The SMB address the ASIC responds to is determined at reset time. After an EEPROM load has completed (due to hardware or software reset or the Main Power Good signal transition to low), TDATA[2:0] are internally latched and are inputs during an EEPROM load and reset. The TDATA[2:0] lines are multiplexed with the SMB address lines 2 through 0 (SMB_A[2:0]). The value of these input pins, SMB_A[2:0], are used to create the SMB address of 0101XXXb, where XXX represents SMB_A2, SMB_A1, and SMB_A0, respectively. These inputs can be configured using pull-up or pull-down resistors. There are default pull-up and pull-down resistors in the silicon to select 110b on SMB_A[2:0]. However, the internal pull-up resistors in the device for the SMB address are too weak; therefore, all ones for SMB address lines require a strong, external pull-up resistor (for example, a value of 2 KΩ). Resistor values and tolerances are described in Section 6.0, “Electrical Specifications” on page 27.

More details on SMB can be found in the *Intel System Management Bus Specification, Revision 1.0*.

For register accesses to the Alert on LAN ASIC, a simple set of SMB commands are supported: Write Byte command and Read Byte command. The command field can be used to access the individual registers.

Explicit details on the SMB cycles and bit definitions are described in Section 4.0, “Configuration and Status Registers” on page 17.

The SMB interface can be configured to drive the SMB Data Input/Output and SMB Serial Clock pins low when the Main Power Good signal equals 0b by using the Drive SMB bit of the Control register. This is one method of preventing the open drain bus from floating when other SMB connections have been powered-off. After reset, the SMB interface will be driven low if the Main Power Good signal equals 0b until the Control register is read. At this point, the function will depend on the configuration bit. It requires approximately 125 microseconds from reset to read the Drive SMB bit in the Control register.

2.3 EEPROM Interface

Note: The Alert on LAN ASIC requires a 64x16 EEPROM which is separate from the 82558B's EEPROM.

The EEPROM interface is provided to allow default configuration information. This gives the Alert on LAN ASIC a default power-up state of enabled and disabled events, IP packet information, Individual Address, and other configuration data.

The Alert on LAN ASIC reads information from the EEPROM during the following:

- **Hardware Reset**. This happens when the Alert on LAN ASIC is first powered-up or when the Auxiliary Power Good (AUX_GOOD) signal transitions low. The Alert on LAN ASIC begins loading the EEPROM configuration information as soon as reset is de-asserted.
- **Software Reset**. This is accomplished by writing to bit 7 of the Test Mode register via the SMB. After reset has completed, the Alert on LAN ASIC begins reading the EEPROM.
- **Hard Transition to G2 Power State**. A hard transition to the G2 power state occurs when the system is powered down before software notifies the Alert on LAN ASIC of the transition by

setting the ACPI State Indicator in the Control register equal to 10b, where the value of 10b indicates that the system is in the G2 power state. This typically occurs when the system is powered down using the 4-second power switch. Loading the EEPROM at this time guarantees that the Alert on LAN ASIC is placed in a known state since the sudden power loss occurred without software knowledge.

The Alert on LAN ASIC reads the first 62 words (124 bytes) of the data in the EEPROM and leaves the last two words (4 bytes) free for vendor information. To ensure that the EEPROM contains valid data, the Alert on LAN ASIC uses word 3Dh as a checksum. The checksum is a 16-bit value that causes the sum of all of the ASIC's data and checksum (in other words, words 00h through 3Dh) to be equal to BABAh. If the checksum is invalid, the ASIC resets most of its registers to the reset value to prevent it from entering an unpredictable state due to invalid EEPROM data.

The reset values for the registers are such that all packet transmissions and SMI events are disabled until the EEPROM is loaded. SMB writes should also be prevented by software during an EEPROM load. SMB reads are always permitted and should be used to check the EEPROM Read Complete Indication bit in the EEPROM Access register (Section 4.14, "Register Ch; EEPROM Access" on page 23) to determine when the EEPROM load has completed.

The EEPROM interface is a MicroWire** interface that uses 4 control signals: EEPROM Chip Select (EECS), EEPROM Serial Clock (EESK), EEPROM Data Input (EEDI) and EEPROM Data Output (EEDO). More details on the MicroWire interface can be found in a MicroWire EEPROM datasheet.

A GPIO interface is provided to access the EEPROM from software. This allows each EEPROM bit to be controlled through the SMB register interface. This is the only method in which the EEPROM can be programmed.

2.4 Event Interface

2.4.1 New Event Definition and Results

There are two components of the event interface. The first portion is the occurrence of an event. An event occurrence happens any time an event is caused: an event pin is at the active level, a software event is set via an SMB write, or the Watchdog Timer expires. If the EEPROM does not load, each of these events will be set in the Event Status register when they happen.

The second part of the event interface is a *new event*. The term new event refers to any event occurrence that initiates a new packet to be generated and transmitted, regardless of whether a packet is currently being transmitted or not. A new event occurs whenever one of the following happens:

- A bit in the Event Status register changes from inactive to active and the Event Mask register bit is already enabled for this event. This occurs any time an unmasked event becomes active and the status bit was previously 0b, either because the event did not happened before or because software cleared it.
- The Event Status register is already set for a particular event, and the Event Mask is changed from inactive to active. Since an event that occurs is stored in the Event Status register, the event does not have to be currently active in order to produce a new event.
- For a Software Event, a new event occurs whenever software writes a 1b to the Software Event Status bit in the Event Status register.

All of the above are considered new events because they initiate a new packet transmission and interrupt any current transmissions. Section 2.4.9, “New Event Packet Transmissions” on page 9 describes new event occurrences in more detail.

Note: A heartbeat does not cause a new event. Although it can initiate a packet, it does not interrupt current packet transmissions. If it does initiate a packet, the Quantum field will be incremented for that new packet. If the heartbeat occurs within the new event packet transmission window (three packets including the time period between the three packets), the current heartbeat will be ignored. The other reason that a heartbeat is not a new event is because it only causes a single packet to be transmitted, rather than three.

2.4.2 External Events

The external events are level inputs that cause alert packets to be sent by the Alert on LAN ASIC. The active level (polarity) of the signals is configurable through the Polarity register, which is written to by the EEPROM and SMB writes. Each hardware event is latched in the Event Status register after it has occurred, regardless of the Event Mask or SMI Mask registers. To clear the event and SMI, if enabled, a 1b must be written to the appropriate status register bit.

The Event Mask register selects the events that can cause an alert packet transmission as well as masking the status bits into the packet payload. The SMI Mask register selects the events that can cause an SMI event. Both of these registers are loaded by the EEPROM and are configurable through the SMB interface.

Every time a new event is activated, the Alert on LAN ASIC sends an alert as soon as possible (the 82558B can invoke wait states). At the same time, the retransmission timer starts. At the expiration of this timer, a second identical packet is sent followed by a third packet after the same timer interval. Whenever a new event is activated, this sequence begins again. The ASIC does not continually send alert packets while the level input is active. This helps reduce the amount of redundant management and network-generated traffic.

Alert packets always take priority over heartbeat packets. If an event occurs, three alert packets are sent along with the retransmission delays before another heartbeat packet is sent.

The Retransmission Timer starts when the packet is queued to be transmitted. If the packet has not been transmitted by the time the retransmission timer has expired, the next packet will not be transmitted. This is highly unlikely to occur; however, it is possible if the 82558B delays the transmission of the packet. Possible delays may include an EEPROM read or collision back-off.

There are five separate external level events:

1. **Cover Tamper**. This indicates that the cover has been opened or tampered with.
2. **Environmental SMI**. This indicates that the environmental control IC has generated an SMI event.
3. **BTI Temperature**. This indicates that the environmental control IC has generated an SMI event.
4. **LAN Leash**. This indicates that the LAN has lost its link. This event signal uses a different interface than other events. If enabled, the detection of a link that has been down for five to ten seconds generates an event; however, the Alert on LAN ASIC does not transmit unless the link is currently valid.
5. **Processor Missing**. This indicates that the processor is not installed.

Although these events are defined, they can be used for any event as long as the corresponding software can function properly.

2.4.3 Event 1, Sticky Latch Clearing Mechanism

The Event_1 input signal to the Alert on LAN ASIC is designed to work with an event that is stored in a sticky latch. This event can be configured to clear the sticky latch by driving the opposite polarity on the Event_1 pin. If configured, this will occur when the Event Status register for Event_1 is cleared by writing a 1b to this bit. The Alert on LAN ASIC will drive the Event_1 signal for a minimum of 20 ms, allowing plenty of time for the sticky latch to clear. Section 8.0, “Appendix A: Alert on LAN Supporting Hardware” on page 31 describes the sticky latch in more detail.

With the exception of the sticky latch clearing mechanism, the Event 1 input behaves similar to the other events. To enable the clearing mechanism of the Event 1 input, the POL_CLREV1 bit of the Polarity register must be set. If it is desired not to use a sticky latch on Event 1, the clearing mechanism can be disabled by clearing the POL_CLEV1 bit.

2.4.4 Event 4, Link Detect and Packet Transmission Interrupt

The Event 4 input is designed for use with the Link status output from the 82558B. There are two special enable functions available with this event.

First is the method of detecting a lost link. If configured, the Alert on LAN ASIC will only cause an Event 4 in the Event Status register if it detects an inactive link (based on polarity setting) for two consecutive timer ticks separated by 5.4 seconds. The window of time that the event will detect link loss is between 5.4 through 10.8 seconds since the “tick time” and “link loss” events are not synchronous to each other. This feature is required to prevent events on PHY resets and 82558B resets, which should produce an invalid link for approximately 3 seconds.

The second feature of the Event_4 input signal is its ability to cancel or disable packet transmissions across the TCO interface whenever the Event_4 pin is active. An active event on Event_4 indicates that link is down, which will obviously prevent packet transmission on the network, even though the TCO transaction may be successful. Any packet currently being transmitted will be interrupted and retransmission will occur when link returns.

The above two features cause the Event_4 input to cause the Alert on LAN ASIC to behave differently than it would for other events. In order to activate these features, the POL_LNKEV4 bit in the Polarity register must be set. If it is desired not to use these features, this bit must be disabled.

Since link is always lost when power is completely off (G3 state), this event is preset in the Event Status register, causing a new event (if the Event Mask is set appropriately) when the Alert on LAN ASIC is powered up.

Note: A software reset will not preset or clear this bit. If this feature is not desired, then the Event_4 Status bit can be cleared before the mask is enabled.

2.4.5 Watchdog Event

The Watchdog event is similar to other events, except that it is caused by an internal timer expiring. The Watchdog event can be used to notify the network console when the monitored machine hangs during boot-up. For example, the timer can be set and enabled upon initial power-up. If the system reaches a specified point during boot-up, BIOS can disable the Watchdog Timer, preventing a Watchdog event. If the system hangs before this point in boot-up is reached, the Watchdog Timer will time-out and notify the network console.

Since a hard G2 transition can happen without software knowledge, it is important to disable watchdog events during G2. This is done by temporarily disabling the watchdog enable while the PWR_GOOD signal equals 0b. This disables the Watchdog Timer during G2, and if a hard G2 transition occurs, an EEPROM load will reload the Watchdog Timer and possibly set it to be enabled. At the point that the PWR_GOOD signal transitions high, the Watchdog Timer becomes enabled (if configured to be enabled) and starts counting from its initial loaded value, essentially restarting the boot-up time-out timer.

2.4.6 Software Event

The software event also has unique functionality due to its special purpose. The event status bit is set when a 1b is written to the Software Status Event bit of the Event Status register. After three packets have been transmitted successfully, this bit is cleared in the Event Status register. However, a write of 1b at any time to this bit will cause a new event and cause the ASIC to start transmitting a new series of event packets with the current software information. Software can detect which packet is in progress by monitoring the CTL_RTCNT bits of the Control Register.

2.4.7 Polarity Functionality

For the six external events, the Event Polarity register informs the Alert on LAN ASIC whether a particular event is active high or low. The top two bits of the Event Polarity register enable the special features available for Events 1 and 4 (described above).

2.4.8 Event Status Mask and SMI Mask

The Event Mask register selects the events that can cause an SOS packet transmission as well as masking the status bits into the packet payload. The SMI Mask selects the events that will cause an SMI. Both of these registers are loaded by the EEPROM and configurable through the SMB interface.

While the EEPROM is being read, no events will be observed by the Alert on LAN ASIC, regardless of either of the mask settings. After the EEPROM is finished loading, the Alert on LAN ASIC allows the events to enter into the status register, subsequently causing a packet to be sent or the SMI output to be asserted depending on the setting of the mask registers.

2.4.9 New Event Packet Transmissions

Every time a new event occurs, the following sequence of events will be performed:

1. Any current packet transmission will be aborted.
2. The Quantum counter will increment.
3. The CTL_RTCNT counter value will be reset to 11b.
4. The Retransmission Timer will be reloaded.
5. Data is latched internal to Alert on LAN ASIC for packet creation:
   - — High byte of Quantum counter
   - — Low byte of Quantum counter
   - — Masked Event Status register
   - — Control register (since it is latched, all 3 packets will show RTCNT equals 11b)

— High byte of Software register

— Low byte of Software register

— Watchdog data

6. The UDP checksum word will be incrementally calculated based on the data above and written at the appropriate UDP checksum location.
7. Assuming that a packet can be sent (CTL_TXEN is set, the EEPROM has completed loading, 82558_RST is not active, TREADY# is not active or the CTL_TRDY is clear, and link is valid or POL_LNKEV4 is clear), the complete packet, internally latched, will be transmitted to the 82558 via the TCO bus.
8. Once the packet has been successfully transmitted to the 82558B, the CTL_RTCNT counter will be decremented one. The sequence is 11b, 10b, 01b, 00b.
9. When the Retransmission timer is expired, execution will begin at step 7 if the CTL_RTCNT counter value does not equal 00b. If CTL_RTCNT equals 00b after the previous packet has been transmitted (3 identical packets have been transmitted), then packet transmissions stop until the next new event or a heartbeat occurs.

Since this process is always restarted when a new event occurs, it is possible to skip Quantum numbers on the network transmissions. For example:

- Event A occurs and causes 3 packets with Quantum *n* to transmit.
- Event B occurs and starts transmitting 1 packet with Quantum *n+1*.
- Event C occurs in the middle of the packet from Event B.

  This causes this packet transmission to halt, and a new packet is started with Quantum *n+2*. Therefore, the packet with Quantum *n+1* is never actually fully transmitted.

Note: SOS alerts will always take priority over heartbeat packets. If an event occurs, three SOS packets will be sent along with the re-transmission delays before another heartbeat packet is transmitted.

2.5 Event Timers

The Event Timers consist of a clock divider circuit and three timers within the Alert on LAN ASIC:

1. **Heartbeat Timer**. This timer controls the heartbeat status packet frequency. The Alert on LAN ASIC transmits one packet per heartbeat timer expiration.
2. **Watchdog Timer**. This is a configurable timer used to time-out on critical events (for example, failed OS boot, POST failure, OS hang, etc.).
3. **Retransmission Timer**. This timer controls the frequency of the retransmission of SOS packets. The Alert on LAN ASIC transmits an alert packet three times.

The Watchdog Timer Event is automatically masked by hardware while the Main Power Good signal equals 0b. This prevents the Watchdog Timer from failing when system power is lost. The Watchdog Timer is used only to detect an OS hang.

2.6 Synchronous RAM and Packet Control

There is a 128-byte synchronous RAM block inside of the Alert on LAN ASIC primarily used for storing the packet to be sent. The contents of the EEPROM are directly loaded into RAM when an EEPROM load occurs. The packet control block is responsible for adding TCO data and dynamic packet data to the RAM and controlling the TCO block to send each packet out to the TCO interface.

2.7 Clock Synchronization Logic

The clock synchronization logic is used to provide a smooth transition of clocks for the 82558B. Since the 82558B requires a clock for TCO support in low power states, clock synchronization logic is a necessity. This logic ensures that the transition between the PCI clock and the 25 MHz clock generated by the 82558B is smooth and non-glitching. This assures that the 82558B continues to operate in a known state.

PCI_CK and B25_CK are the PCI and the 82558B 25 MHz output clocks, respectively. The Alert on LAN ASIC must monitor both in order to provide a smooth transition between both clocks. Both clocks are required during the power state transition (in other words, PWR_GOOD transitions low). after the Main Power Good signal transitions low at least 3 PCI clocks are required to switch from the PCI clock to the 82558B's 25 MHz clock.

PCI_SEL and B25_SEL are the PCI and the 82558B 25 MHz clock gates, respectively. These outputs control analog switches that can turn the clocks on or off.

Note: The analog switches used must be selected carefully to guarantee that the PCI clock skew specifications are not violated.

2.8 SMI Logic

The SMI# signal is asserted (active low) if the Event Status and the SMI Mask bits are set for any particular event, with the exception of a software event. The software event cannot be used to generate an SMI.

Since the SMI# requires both the Event Status and the SMI mask for one event to be set, clearing any one of these two bits will de-assert the SMI# signal if it is the only event causing the SMI#.

If one external event has occurred and the SMI mask bit is set, the SMI# signal will be active. If the event is cleared by writing a 1b to the appropriate status bit, the event will be cleared in the Alert on LAN ASIC. However, if the event is still active, it will be set again in the Event Status register. The net result is that the SMI# line will pulse inactive for a single 25 MHz clock cycle. If this is undesired, software will need to take steps to avoid this. This can be achieved by disabling the SMI mask bit or ensuring that the external event is no longer active.

SMI events can happen independently or jointly with packet transmission events since each has its own SMI Mask register.

2.9 Miscellaneous Logic

The Alert on LAN ASIC has a block of miscellaneous logic, consisting of registers, reset circuitry, and PWR_GOOD monitoring. The power monitoring is significant and explained in this section.

The Alert on LAN ASIC monitors two input signals, PWR_GOOD and AUX_GOOD, to indicate the status of the main power supply and the auxiliary power supply, respectively. These signals allow the Alert on LAN ASIC to determine the state of the power supplies and control the 82558B appropriately. This enables the Alert on LAN ASIC to determine whether or not the PCI interface is active.

In order to guarantee that ALTRST# is asserted before ISOLATE#, the Alert on LAN ASIC provides the combinational logic driven by PWR_GOOD and AUX_GOOD to control the ISOLATE# output. This is important since the 82558B will not be able to propagate a reset unless four clock cycles are present while ALTRST# or PCI_RST# is active and ISOLATE# is inactive.

Another main function of the Alert on LAN ASIC is to determine when power has been lost or attained to the main power plane. This allows the Alert on LAN ASIC to enable or disable certain events as necessary for the different power states.

The Alert on LAN ASIC monitors the Main Power Good signal at all times and is designed to detect when the system has been powered down with or without software knowledge. When the system is powered down normally, software will set the ACPI state in the ACPI State Indicator bits of the Control register to ACPI G2 state (10b), anticipating a power-down. From this state, the Alert on LAN ASIC will continue operating normally if the system is powered down (for example, the Main Power Good signal transitions from high to low). However, if the ACPI system state is not set to G2 when the Main Power Good signal transitions from high to low, the Alert on LAN ASIC will force a re-read of the EEPROM to load its default values. This ensures that the Alert on LAN ASIC will be able to operate in a known state, rather than an unpredictable state due to the software unaware power-down.

PCI_RST# is used as an input to the Alert on LAN ASIC and as a stimulus to reset the 82558B with the 82558_RST# signal. In a system with the Alert on LAN management solution, it is undesirable to reset the 82558B while the Main Power Good signal is low. The Alert on LAN ASIC only allows PCI_RST# to assert 82558_RST# when the Main Power Good signal is 1b. This input can also cause the Alert on LAN ASIC to terminate any TCO transactions with the 82558B until it can continue at a later time. The Alert on LAN ASIC offers software the capability of resetting the 82558B through the use of the CTL_558RST bit in the Control register (Section 4.11, “Register 9h; Control” on page 22).

The Main Power Good signal effect on the propagation of PCI_RST# to 82558_RST# is important since PIIX4 will assert a PCI_RST# when power is being lost. However, PCI_RST# will reset the 82558B which is undesirable. Therefore, the Alert on LAN ASIC uses the Main Power Good signal to determine if PCI_RST# should be propagated or not. This assumes that the Main Power Good signal is de-asserted before PCI_RST#.

3.0 Signal Description

3.1 Signal Type Definition

Symbol	Name	Description
I	Input	Input is a standard input.
O	Totem Pole Output	Totem pole output is a standard active driver.
I/O	Input/Output	This signal is used for input and output to the device.
OD	Open Drain	Open drain allows multiple devices to share as a wired OR gate.
CMOS	CMOS Input Buffer	Voltage detail for the CMOS Input Buffer are described in Section 6.3, "DC Characteristics" on page 27.
TTL	TTL Input Buffer	Voltage detail for the CMOS Input Buffer are described in Section 6.3, "DC Characteristics" on page 27.
S	Schmitt-Trigger Input	This is used as Schmitt-Trigger Input.
PU	Pull-up Resistor	Pull-up resistance in the silicon is present.
PD	Pull-down Resistor	Pull-down resistance in the silicon is present.
n mA		Output buffer drive in milliamps, where *n* is an integer value.

3.2 Clock Signals

Symbol	Pin	Type	Name and Function
PCI_CK	40	I, PD, CMOS	**PCI Clock.** This signal is the PCI clock from the PCI interface. The frequency range is 0 to 33 MHz.
B25_CK	42	I, CMOS	**82558 Generated Clock.** This is a 25 MHz clock input provided by the 82558B. This clock is expected to operate at all times at a constant 25 MHz frequency, unless power to the Alert on LAN ASIC is lost.
PCI_SEL	41	O, 6 mA	**PCI_CK Select.** This pin is asserted high (active) when PCI_CK is enabled to the 82558B.
B25_SEL	43	O, 4 mA	**B25_CK Select.** This pin is asserted high (active) when B25_CK is enabled to the 82558B.

3.3 SMB Interface Signals

Symbol	Pin	Type	Name and Function
SMB_SCL	36	I/O, OD, TTL, S, 4 mA	**SMB Serial Clock.** This pin is the clock signal provided by the system in order to communicate over SMB. This pin is used as output when driven low during reset and while PWR_GOOD is equal to 0b if enabled (Drive SMB bit in the Control register). Otherwise, the SMB_SCL signal is used as input.

Symbol	Pin	Type	Name and Function
SMB_SDA	37	I/O, OD, TTL, S, 4 mA	**SMB Data Input/Output.** This pin is the data signal used to transfer data over the SMB. It is used as output when driven low during reset and while PWR_GOOD is equal to 0b if enabled (drive SMB bit in the Control register). Otherwise, the SMB_SDA signal is used as input and output for SMB data.

3.4 82558 B-step Flash Interface Signals

Symbol	Pin	Type	Name and Function
TDATA7 (TEST_EN)	13	I/O, PU, CMOS, 2 mA	**TCO Data Bus [7].** During reset (AUX_GOOD = 0b), this pin acts as the Test Enable (TEST_EN) input. On the rising edge of reset, the test enable is latched and active. A high value causes the test mode to be enabled. Otherwise, TDATA7 is used for the TCO data bus.
TDATA6 (TEST_MODE)	12	I/O, PU, CMOS, 2 mA	**TCO Data Bus [6].** During reset (AUX_GOOD = 0b), this pin acts as the TEST_MODE input. On the rising edge of reset, the test mode is latched and active. Otherwise, TDATA6 is used for the TCO data bus.
TDATA5 TDATA4 TDATA3	9 8 7	O, 2 mA	**TCO Data Bus [5:3].** The data bus is used to transmit packets from the Alert on LAN ASIC to the 82558B. This data is only valid when the TFORCE signal is asserted.
TDATA2 TDATA1 TDATA0 (SMB_A[2:0])	4 3 2	I/O, PU/ PD, CMOS, 2 mA	**TCO Data Bus [2:0].** During reset and EEPROM load, these pins act as inputs. At the end of an EEPROM load, the SMB address is latched and TDATA[2:0] acts as output for SMB_A[2:0]. The default address is 110b via internal pull-up and pull-down resistors. Otherwise, TDATA[2:0] is used for the TCO data bus.
TMARKER	11	O, 2 mA	**TCO Marker.** The marker strobe is used to indicate the start and end of a TCO command on the TDATA[7:0] bus. When TMARKER is active, this indicates that TDATA contains a TCO command byte (not a data byte).
TRDREQ	14	O, 2 mA	**TCO Read Request.** When TRDREQ is asserted (active high), it indicates that the Alert on LAN ASIC has one byte to be transferred to the 82558B. TRDREQ is de-asserted upon acknowledgment from the TACTIVE signal.
TACTIVE	1	I, CMOS	**TCO Active.** TACTIVE is asserted by the 82558B to indicate that the 82558B has acknowledged a TRDREQ transaction (TFORCE = 1b) or that the 82558B is not ready for a TCO cycle (TFORCE = 0b).
TFORCE	44	O, 2 mA	**TCO Force.** TFORCE is a control signal used to force the 82558B into TCO mode. When the 82558B is forced into TCO mode, the TDATA[7:0] and TMARKER interface on the 82558B is activated.
TSTATUS#	10	I, CMOS	**TCO Status.** TSTATUS# is an active low input indicating that the 82558B has completed its current TCO command. This indication is necessary to mark the end of packet transmission.
TREADY#	35	I, CMOS	**TCO Ready.** The TCO Ready signal is an active low input indicating the power state of the 82558B. If it is asserted, the 82558B is in a low power state (D1, D2, or D3). This input indicates when the Alert on LAN ASIC should de-assert the TFORCE signal in wake-up scenarios

3.5 EEPROM Interface Signals

Symbol	Pin	Type	Name and Function
EE_CS	18	O, 1 mA	**EEPROM Chip Select.** EEPROM Chip Select is used to control access to the EEPROM.
EE_SK	19	O, 1 mA	**EEPROM Shift Clock.** The EE_SK signal is used to shift data in and out of the EEPROM.
EE_DO	21	I, TTL, PU	**EEPROM Data Out.** Serial data output from the EEPROM.
EE_DI	20	O, 1 mA	**EEPROM Data In.** Serial data input to the EEPROM.

3.6 Alert/SOS Events Signals

Symbol	Pin	Type	Name and Function
EVENT_1	22	I/O, TTL, S, 4 mA	**Event_1 - Cover Tamper.** Level input that causes alert 1 packet transmission. This pin can be used as output as a clearing mechanism on external sticky logic.
EVENT_2	23	I, TTL, S	**Event_2 - ENV_SMI.** Level input that causes alert 2 packet transmission.
EVENT_3	24	I, TTL, S	**Event_3 - BTI_Temperature.** Level input that causes alert 3 packet transmission.
EVENT_4	25	I, TTL, S	**Event_4 - LANLeash.** Level input that causes alert 4 packet transmission.
EVENT_5	26	I, TTL, S	**Event_5 - Processor Missing.** Level input that causes alert 5 packet transmission.
Reserved	29	N/A	This pin is reserved and should be pulled down to 0b via a 220Ω resistor.

3.7 Miscellaneous Signals

Symbol	Pin	Type	Name and Function
PCI_RST#	32	I, TTL	**PCI Reset.** The PCI_RST# pin is an active low input signal from the PCI interface. It propagates to the 82558B through the 82558_RST# line if PWR_GOOD is active. It is also used as an indication to the Alert on LAN ASIC that the 82558B is being reset.
82558_RST#	15	O, 2 mA	**82558 Reset.** The 82558 Reset signal is an active low reset. It is driven when the PCI_RST# signal is active and the PWR_GOOD signal is active. It is also driven when an 82558B software reset is triggered through the internal registers.
ISOLATE#	33	O, 2 mA	**Isolate Output.** This output signal is used to isolate the PCI bus on the 82558B. It implements the 82558B Wake on LAN* (WOL) circuitry to guarantee that the ALTRST# signal of the 82558B is asserted before ISOLATE# is asserted. This is based on the PWR_GOOD and AUX_GOOD signals.
SMI#	34	O, OD, 2 mA	**SMI Output.** The SMI# signal is asserted by the Alert on LAN ASIC for various events depending on the SMI mask register settings. SMI# is de-asserted by clearing the events or masks in the Alert on LAN ASIC's status registers.

3.8 Power and Ground Signals

Symbol	Pin	Type	Name and Function
PWR_GOOD	31	I, TTL, S	**Main Power Good.** This signal indicates that the main +5 V power supply is available.
AUX_GOOD	30	I, TTL	**Auxiliary Power Good.** This signal indicates that an auxiliary power supply is available. It is also used as an active low reset to the Alert on LAN ASIC.
VDD	5, 16, 27, 38		**Power.** +5 V ± 5%
GND	6, 17, 28, 39		**Ground.** 0 V

4.0 Configuration and Status Registers

The Alert on LAN ASIC configuration and status registers are accessible through the SMB. The SMB cycles for register reads and writes are shown below.

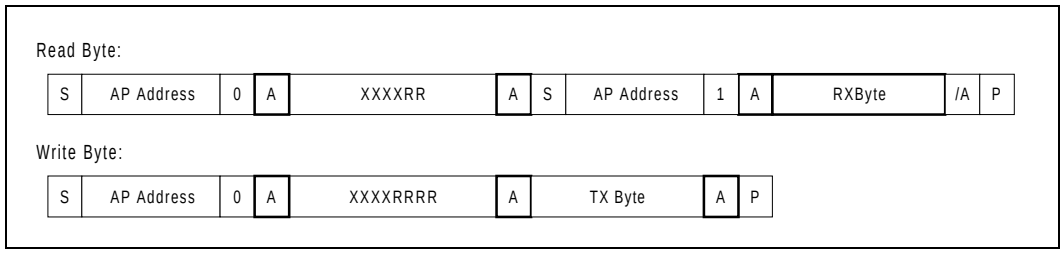

Figure 2. SMB Register Read and Write Cycle

4.1 Register Bit Types

Symbol	Description
R/W	Read/Write
RO	Read Only
SC	Self Clearing
R/W1	Read/Write 1b to clear
EE(*x*)	Default value from EEPROM with a value of '*x*' if the EEPROM is invalid
HWRST	Hardware Reset only (software reset has no effect)

4.2 Register 0h; Revision ID

The Revision ID register identifies the Alert on LAN ASIC and its silicon revision. It is intended to provide software a method of accessing this information.

Bits	Name	Type	Name and Description	Default
7:3	AP_ID	RO	**Alert on LAN ID.** This register contains the 11010b binary code identifying the Alert on LAN ASIC.	11010b
2:0	AP_REV	RO	**Alert on LAN Silicon Revision.** This register contains the three bit coded silicon revision.	XXXb

4.3 Register 1h; Event Status

The Event Status register holds the status of all events. The watchdog event and events one through five are set when the event occurs and remain set until software clears them by writing a 1b to the event status bit. The Software Event, bit 7, is set via software causing an event and self-clears after three packet transmissions. However, writing a 1b to the Software Event bit always causes a new packet to be started, regardless of how many packets have been transmitted. If software wants to send only one packet before it causes a new Software Event, it may monitor the packet retry counter in the Retransmission Count field (CTL_RTCNT) in the Control register. When STA_EV1

is cleared by writing a 1b to bit 0 and the Clear Sticky Latch Polarity bit (POL_CLREV1) in the Event Polarity register equals 1b, the EVENT_1 pin outputs the opposite of the Event Polarity register bit between 20 and 40 milliseconds.

Bits	Name	Type	Name and Description	Default
7	STA_SWE	R/W SC	**Software Event Status.** This bit is set if software causes an event. It can also be forced by writing a 1b to this bit. 1 = Force Software Event This bit self-clears after three software event packet transmissions.	0b
6	STA_WDG	R/W1	**Watchdog Event Status.** This bit is set if the Watchdog Timer has expired. Writing a 1b to this bit clears it. 1 = Watchdog Timer expired	0b
5	Reserved		This bit is reserved and should be set to 0b.	0b
4	STA_EV5	R/W1	**Event_5 Status.** This bit indicates status of Event 5, Processor Missing. It is set if the processor is not installed. Writing a 1b to this bit clears it. 1 = Event_5 occurred	0b
3	STA_EV4	R/W1	**Event_4 Status.** This bit indicates status of Event 4, LAN Leash. It is set if the LAN has lost its link. Writing a 1b to this bit clears it. 1 = Event_4 occurred	1b[a]
2	STA_EV3	R/W1	**Event_3 Status.** This bit indicates status of Event 3, BTI Temperature. It is set if the BTI temperature is out of the specified range. Writing a 1b to this bit clears it. 1 = Event_3 occurred	0b
1	STA_EV2	R/W1	**Event_2 Status.** This bit indicates status of Event 2, ENV_SMI. It is set if the hardware monitoring device has an SMI event. Writing a 1b to this bit clears it. 1 = Event_2 occurred	0b
0	STA_EV1	R/W1	**Event_1 Status.** This bit indicates status of Event 1, Cover Tamper. It is set if the cover has been opened or tampered with. Writing a 1 to this bit clears it. 1 = Event_1 occurred	0b

a. A hardware reset causes this bit to return to its default value of 1b; a software reset leaves this bit value unaffected.

4.4 Register 2h; Event Polarity

The Event Polarity register is used to set the polarity of the event inputs. This flexibility allows the Alert on LAN to handle external interfaces that are either active low or active high.

Bits	Name	Type	Name and Description	Default
7	POL_CLREV1	R/W	**Clear Sticky Latch.** This bit enables the EVENT_1 pin to drive out and clear a sticky latch. This bit is enabled when set to 1b.	EE(0)
6	POL_LNKEV4	R/W	**Link Status.** This bit enables the EVENT_4 pin to act as link status input. When it is enabled, the EVENT_4 status is only latched if the event is active for five to ten seconds, and packet transmission is valid only when link is good.	EE(0)

Bits	Name	Type	Name and Description	Default
5	Reserved	RO	This bit is reserved and should be set to 0b.	0b
4	POL_EV5	R/W	**Event_5 Polarity.** 1 = Active High 0 = Active Low	EE(0)
3	POL_EV4	R/W	**Event_4 Polarity.** 1 = Active High 0 = Active Low	EE(0)
2	POL_EV3	R/W	**Event_3 Polarity.** 1 = Active High 0 = Active Low	EE(0)
1	POL_EV2	R/W	**Event_2 Polarity.** 1 = Active High 0 = Active Low	EE(0)
0	POL_EV1	R/W	**Event_1 Polarity.** 1 = Active High 0 = Active Low	EE(0)

4.5 Register 3h; Event Mask

The Event Mask register is used to mask events from transmitting SOS packets. If the event bit is set to 1b, the event will cause an SOS packet. If it is 0b, it will not. This mask also prevents the event from showing up in the status byte in the packet when the bit is 0b.

Bits	Name	Type	Name and Description	Default
7	Reserved	RO	This bit is reserved and should be set to 0b.	0b
6	MSK_WDG	R/W	**Watchdog Event Mask.** 1 = Watchdog Timer packet enabled	EE(0)
5	Reserved	R/W	This bit is reserved and should be set to 0b.	EE(0)
4	MSK_EV5	R/W	**Event_5 Mask.** 1 = Event_5 transmit packet enabled	EE(0)
3	MSK_EV4	R/W	**Event_4 Mask.** 1 = Event_4 transmit packet enabled	EE(0)
2	MSK_EV3	R/W	**Event_3 Mask.** 1 = Event_3 transmit packet enabled	EE(0)
1	MSK_EV2	R/W	**Event_2 Mask.** 1 = Event_2 transmit packet enabled	EE(0)
0	MSK_EV1	R/W	**Event_1 Mask.** 1 = Event_1 transmit packet enabled	EE(0)

Note: The Watchdog event is masked by hardware when the PWR_GOOD signal is low.

4.6 Register 4h; SMI Mask

The SMI Mask register is used to mask events from causing an System Management Interrupt (SMI). If the event bit is set to 1b, the event will cause an SMI. If it is set to 0b, it will not.

Bits	Name	Type	Name and Description	Default
7	Reserved	RO	This bit is reserved and should be set to 0b.	0b
6	SMI_WDG	R/W	**Watchdog Event SMI Mask.** 1 = Watchdog Timer SMI enabled	EE(0)
5	Reserved	R/W	This bit is reserved and should be set to 0b.	0b
4	SMI_EV5	R/W	**Event_5 SMI Mask.** 1 = Event_5 SMI enabled	EE(0)
3	SMI_EV4	R/W	**Event_4 SMI Mask.** 1 = Event_4 SMI enabled	EE(0)
2	SMI_EV3	R/W	**Event_3 SMI Mask.** 1 = Event_3 SMI enabled	EE(0)
1	SMI_EV2	R/W	**Event_2 SMI Mask.** 1 = Event_2 SMI enabled	EE(0)
0	SMI_EV1	R/W	**Event_1 SMI Mask.** 1 = Event_1 SMI enabled	EE(0)

4.7 Register 5h; Watchdog Status Byte

The Watchdog Status Byte register is used to provide more watchdog information to the packet recipient. It provides a means of identifying the cause of the watchdog event (such as OS hang, failed boot, etc.). This byte is transmitted with each packet. Note that some software implementations may use this byte as additional information for a software event. This requires that the watchdog event is disabled (masked) during these transmissions since this byte is designated for watchdog data when the watchdog event bit is set in the Event Status register.

Bits	Name	Type	Name and Description	Default
7:0	WDG_DAT	R/W	**Watchdog Status.** This register is byte-wide and indicates the status for transmitted SOS packets on Watchdog Timer expiration.	EE(40h)

4.8 Register 6h; Watchdog Timer

The Watchdog Timer register is used to enable and configure the time-out value of the Watchdog Timer. The watchdog time-out value can only be written to when the timer is disabled. However, the value can be written and the timer enabled in a single SMB write.

The timer begins counting down from the value received during a write to the register. When the timer reaches zero, a new event is caused and the timer begins counting down again. Any write to this register while it is enabled will reload the time-out value. A read from the register will result in the current value of the timer.

Bits	Name	Type	Name and Description	Default
7:1	WDG_VAL	R/W	**Watchdog Timer Value.** This value loads in 43-second resolution with a range from 43 seconds to 92 minutes. It can only be written to while the timer is disabled. This timer has an accuracy of its value minus one tick, where one tick is equal to 43 seconds.	EE(0000001b)
0	WDG_ENA	R/W	**Timer Enable.** 1 = Enable/Reset counter 0 = Disable counter	EE(0)

Note: It is not recommended to set the time-out value to 00h. Although an event will not be caused immediately, one will be caused at the first incident if the timer is loaded with a nonzero value and enabled with one SMB write.

4.9 Register 7h; Heartbeat Timer

The Heartbeat Timer register is used to enable and configure the time-out value of the Heartbeat Timer. The heartbeat time-out value can only be written when the timer is disabled. However, the value can be written and the timer enabled in a single SMB write.

The timer begins counting down from the value received during a write to the register. When the timer reaches zero, a heartbeat event is caused and the timer begins counting down again. Any write to this register while it is enabled reloads the time-out value. A read from the register results in the current value of the timer.

Bits	Name	Type	Name and Description	Default
7:1	HBT_VAL	R/W	**Heartbeat Timer Value.** This value loads in 43-second resolution with a range from 43 seconds to 92 minutes. It can only be written to while the timer is disabled. This timer has an accuracy of its value minus one tick, where one tick is equal to 43 seconds.	EE(0000001b)
0	HBT_ENA	R/W	**Timer Enable.** 1 = Enable/Reset counter 0 = Disable counter	EE(0)

Note: It is not recommended to set the time-out value to 00h. Although an event will not be caused immediately, one will be caused at the first incident if the timer is loaded with a nonzero value and enabled with one SMB write.

4.10 Register 8h; Retransmission Timer

The Retransmission Timer register is used to configure the time-out value of the Retransmission Timer. The Retransmission Timer is always enabled and is reloaded when a new event occurs. Unlike the Watchdog Timer and Heartbeat Timer, the Retransmission Timer only reloads the time-out value when it expires or a new event occurs, not every time a write is done.

Bits	Name	Type	Name and Description	Default
7:1	RTM_VAL	R/W	**Retransmit Timer Value.** This value loads in 2.7-second resolution with a range from 2.7 seconds to 5.7 minutes. It can only be written to while the timer is disabled. This timer has an accuracy of its value minus one tick, where one tick is equal to 2.7 seconds.	EE(0000001b)
0	RTM_RSVD	RO	This bit is reserved and should be set to 0b.	0b

Note: A read from the Retransmission Timer register results in the current time-out value, not the current timer value.

4.11 Register 9h; Control

The Control register is used to provide miscellaneous control and status functions. The retransmission packet count, TCO interface active indication, and APCI states can be obtained from the Control register. Also, the 82558B can be reset, packet transmission can be enabled or disabled, the behavior of the TREADY# signal can be set, and the ACPI state can be changed through this register.

Bits	Name	Type	Name and Description	Default
7:6	CTL_RTCNT	RO	**Retransmission Count.** These bits indicate which of the three Alert on LAN packet types are currently being processed and sent. 11 = First packet 10 = Second packet 01 = Third packet 00 = No SOS packets	00b
5	CTL_TRDY	R/W	**TREADY# Active.** When this bit is set, TFORCE is de-asserted when TREADY# is asserted high. Otherwise, TREADY# does not affect TFORCE.	EE(0)
4	CTL_558RST	R/W	**82558 Software Reset.** Setting this bit to 1b causes the hardware reset line to be asserted to the 82558B. A 0b value de-asserts the reset.	EE(0)
3	CTL_DRSMB	R/W	**Drive SMB.** Setting this bit to 1b causes the Alert on LAN ASIC to drive the open drain SMB interface while PWR_GOOD is low. If this bit is a 0b, the SMB interface operates as normally expected, regardless of PWR_GOOD.	EE(1)
2	CTL_TXEN	R/W	**Transmit Enable.** This bit enables real time control of all Alert on LAN ASIC transmission. When active (1b), transmission occurs as normal; otherwise, when inactive (0b), transmission halts.	EE(0)
1:0	CTL_ACPI	R/W	**ACPI State Indicator.** 00 = G0 Power State 01 = G1 Power State 10 = G2 Power State 11 = Preboot. If the ACPI state is not G2 and PWR_GOOD transitions from high to low, an EEPROM load will occur. Thus, this register is reloaded.	EE(11)

4.12 Register Ah; Software Status Byte 1

The Software Byte 1 register is used to provide detailed software information to the packet recipient. This byte provides a method of sending specific information from the software and is transmitted with each packet. It is intended to be valid when the Software Event bit is set in the Event Status register.

Bits	Name	Type	Name and Description	Default
7:0	SWS1_DAT	R/W	These bits indicate the status of transmitted SOS packets from a Software Event.	00h

4.13 Register Bh; Software Status Byte 2

The Software Byte 2 register is used to provide detailed software information to the packet recipient. This byte provides a method of sending specific information from the software and is transmitted with each packet. It is intended to be valid when the Software Event bit is set in the Event Status register.

Bits	Name	Type	Name and Description	Default
7:0	SWS2_DAT	R/W	These bits indicate the status of transmitted SOS packets from a Software Event.	00h

4.14 Register Ch; EEPROM Access

The EEPROM register is used to give EEPROM status and allow access to the individual EEPROM pins. EEPROM read complete status and invalid checksum status are indicated in this register. A GPIO bit interface is provided to allow software to access and write directly to the EEPROM.

Bits	Name	Type	Name and Description	Default
7	EE_COMP	RO	**EEPROM Read Complete Indication.** This bit is set to 1b after the configuration EEPROM read is complete.	0b
6	EE_ICKSM	RO	**EEPROM Invalid Checksum Indication.** This bit should only be read after the EEPROM read has been completed. 1 = Invalid checksum detected	1b[a]
5:4	Reserved	RO	These bits are reserved and should be set to 00b.	00b
3	EE_DO	RO	**EEDO Input State.** This bit indicates EE_DO status.	Xb
2	EE_DI	R/W	**EEDI Output State.** This bit sets EE_DI status.	0b
1	EE_CS	R/W	**EECS Output State.** This bit sets EE_CS status.	0b
0	EE_SK	R/W	**EESK Output State.** This bit sets EE_SK status.	0b

a. The default value of EE_ICKSM is 1b after reset. After valid data has been detected, EE_ICKSM is set to 0b, valid checksum detected.

4.15 Register Dh; Test Mode

The Test Mode register is used to access internal test modes of the Alert on LAN ASIC and to force a software reset of the ASIC.

Bits	Name	Type	Name and Description	Default
7	TST_RST	R/W SC	**Alert on LAN Software Reset.** This bit is used to reset the Alert on LAN. It performs the equivalent of a hardware reset and re-reads the EEPROM. This bit self-clears and the reset completes after four clock cycles.	0b
6	TST_MODE	R/W	**Test Mode.** The Test Mode enable bit provides access into the Alert on LAN ASIC's Vector Test Mode coverage.	0b

Bits	Name	Type	Name and Description	Default
5	TST_FRC25	R/W	**Force 25 MHz Clock.** This bit forces the clock switching mechanism to select the 82558B 25 MHz generated clock.	0b
4	TST_TCO	RO	**TCO Mode Active Indication.** This bit is active while the Alert on LAN is sending a packet to the 82558B. Otherwise, this bit is cleared.	0b
3	TST_FAST	R/W	**Fast Mode.** The Fast Mode enable bit provides quick test modes for test vector coverage	0b
2:0	Reserved	RO	These bits are reserved and should be set to 000b.	000b

5.0 Reset and Test Modes

5.1 Reset Mode

When the Alert on LAN ASIC's AUX_GOOD signal is asserted (active low), all internal circuits are reset, except for the test mode circuitry. The AUX_GOOD signal is expected to remain low for at least 10 B25_CLK cycles before it is completely reset and stable.

The PCI Reset signal (PCI_RST#) does not reset the Alert on LAN ASIC. However, it is passed through to the 82558 Reset signal (82558_RST#) when PWR_GOOD is active. When PWR_GOOD is de-asserted, the 82558_RST# is driven high (inactive).

5.2 Manufacturing Test Mode

The Alert on LAN ASIC is put into Test Mode when the TDATA7 (TEST_EN) signal, pin 13, is sampled high on the rising edge of reset (AUX_GOOD = 0b). Also, the value of TDATA6 (TEST_MODE) is latched internal to Alert on LAN ASIC. The value of this latched signal determines the test mode that is activated (while TEST_EN is asserted). The two test modes supported are:

- NANDTREE TDATA6 latched value = 0b
- TRI-STATE TDATA6 latched value = 1b

The test mode remains enabled until another reset occurs where TDATA7 is sampled low on the rising edge of reset.

5.2.1 NAND Tree

This test mode provides a NAND tree path around the periphery of Alert on LAN ASIC consisting of all of the Alert on LAN ASIC pin inputs as stimuli.

The first input on the NAND tree is PCI_RST#, pin 32, and the output of the NAND tree is ISOLATE#, pin 33.

The NAND tree travels clockwise around the chip (decreasing pin order), including every input buffer, with the exception of the AUX_GOOD, B25_CLK, and TDATA6 pins.

AUX_GOOD cannot be used as part of the NAND tree because it is used as reset, and B25_CLK has a special input buffer that cannot use the NAND tree. During the test mode, TDATA6 is used as a required dedicated input to the process monitor.

All input buffers are true buffers except for PCI_CLK, which is in inverting input buffer. This should be taken into consideration when implementing the test vectors.

5.2.2 Tri-State

This test mode tri-states all outputs on the Alert on LAN ASIC as well as disables all internal pull-up and pull-down resistors.

5.3 Vector Test Mode

The Alert on LAN ASIC can be put into two different test modes for allowing easier access to registers during testing. By setting TST_MODE in the Test Mode register, the Alert on LAN ASIC provides a special parallel data interface for easy input and output. The ASIC can also be put into a "fast" mode that internally configures the Alert on LAN ASIC such that counters and state machines are free running. This is done by setting the TST_FAST bit in the Test Mode register. These Vector Test Modes are used to provide a method of obtaining better and faster test coverage of internal nodes, helping facilitate higher yields and achieve higher probability of error-free devices on the ASIC manufacturing line. These modes are not recommended in normal operation of Alert on LAN ASIC.

Note: The Vector Test Mode mode will make the Alert on LAN ASIC unusable in its intended operation. These are special modes that are only intended for more efficient test vector coverage.

5.3.1 Vector Input Interface

The input interface to the Vector Test Mode uses 9 bits: 8 bits for data and 1 bit to select between an address phase and a data phase. There is no chip select, which means that an address phase or a data phase will occur at every rising edge of the Alert on LAN ASIC clock.

The 8-bit address/data signals used are TREADY#, EVENT_6, EVENT_5, EVENT_4, EVENT_3, EVENT_2, EVENT_1, and TSTATUS#. The order listed shows the bit order with TREADY# as the most significant bit and TSTATUS# as the least significant bit.

The address/data select input is the TACTIVE signal. When it equals 0b, an address phase occurs on the next rising edge; when the signal is a 1b, a data phase occurs.

The addressing scheme for the input interface is described in Table 1.

Table 1. Vector Input Interface Addressing Scheme

Data Select (TACTIVE)	AD[7:0]	Description
0	1RRRRRRR	This is the address phase where "RRRRRRR" addresses RAM. This allows addressing to all 128 bytes of RAM.
0	0XXRRRRR	This is the address phase where "RRRRR" addresses the Alert on LAN ASIC registers. This addresses up to 32 registers. "XX" are "don't care" bits.
1	DDDDDDDD	This is the data phase where "DDDDDDDD" is the data that is written to the previously latched address from an address phase.

Note: This is only an input interface. Section 5.3.2, "Vector Output Interface" describes the output interface in more detail.

5.3.2 Vector Output Interface

The output interface in Vector Test Mode uses 8 bits. This output bus is simply a result of the current addresses latched from the vector input interface. For example, if the last address phase on the input vector interface was 10001001b, some propagation delay after this value is latched in on the rising clock edge, the output interface would show the results of the RAM, address 09h.

The 8-bit data output signals used are TDATA[7:0]. This order shows the bit order, where TDATA7 is the most significant bit and TDATA0 is the least significant bit.

6.0 Electrical Specifications

6.1 Recommended Operation Conditions

Table 2. Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{DD}	DC voltage supply	4.75	5.25	V
TA	Operating ambient temperature	0	70	C
TJ	Junction temperature		150	C

6.2 Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{DD}	DC voltage supply	-0.3	7.0	V
V_{IN}	Input voltage	-1.0	V_{DD} + 0.3	V
I_{IN}	DC input pin current	-10	10	mA
T_{STG}	Storage temperature	-40	125	C
R_{PUD}	Pull-up/Pull-down resistor	35	65	KΩ

6.3 DC Characteristics

Table 4. DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IL}	Voltage input low	TTL CMOS			0.8 0.2 V_{DD}	V V
V_{IH}	Voltage input high	TTL CMOS			2.0 0.7 V_{DD}	V V
V_T	Switching threshold	TTL CMOS			1.5 2.5	V V
I_{IN}	Input current: CMOS, TTL inputs Inputs with pull-down resistors TTL inputs with pull-up resistors	 $V_{IN} = V_{DD}$ or V_{SS} $V_{IN} = V_{DD}$ $V_{IN} = V_{SS}$	 -10 35 -35	 ±1 115 -115	 10 222 -214	 µA µA µA

Table 4. DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{OH}	Voltage output high	I_{OH} = -1 mA I_{OH} = -2 mA I_{OH} = -4 mA	2.4 2.4 2.4			V V V
V_{OL}	Voltage output low	I_{OL} = 1 mA I_{OL} = 2 mA I_{OL} = 4 mA		0.2 0.2 0.2	0.4 0.4 0.4	V V V
I_{OZ}	Tri-state output leakage current	$V_{OH} = V_{DD}$ or V_{SS}	-10	±1	10	µA
I_{OS}	Output short current[a]	V_{DD} = 5.25 V, $V_O = V_{DD}$; V_{DD} = 5.25 V, $V_O = V_{SS}$	37 -117	90 -75	140 -40	mA mA
I_{DD}	Quiescent supply current	$V_{IN} = V_{DD}$ or V_{SS}		26		mA
C_{IN}	Input capacitance	Any input and bidirectional buffer		2.5		pF
C_{OUT}	Output capacitance	Any output buffer[b]		2.0		pF

a. I_{OS} is a 4 mA output. The output short circuit current for other outputs will scale.
b. Output using single buffer structure (excluding package).

7.0 Packaging Information

Pin allocation is based on a 44-pin Thin Quad Flat Package (TQFP). Package dimensions and its attributes are shown in Figure 3 and Table 5 below.

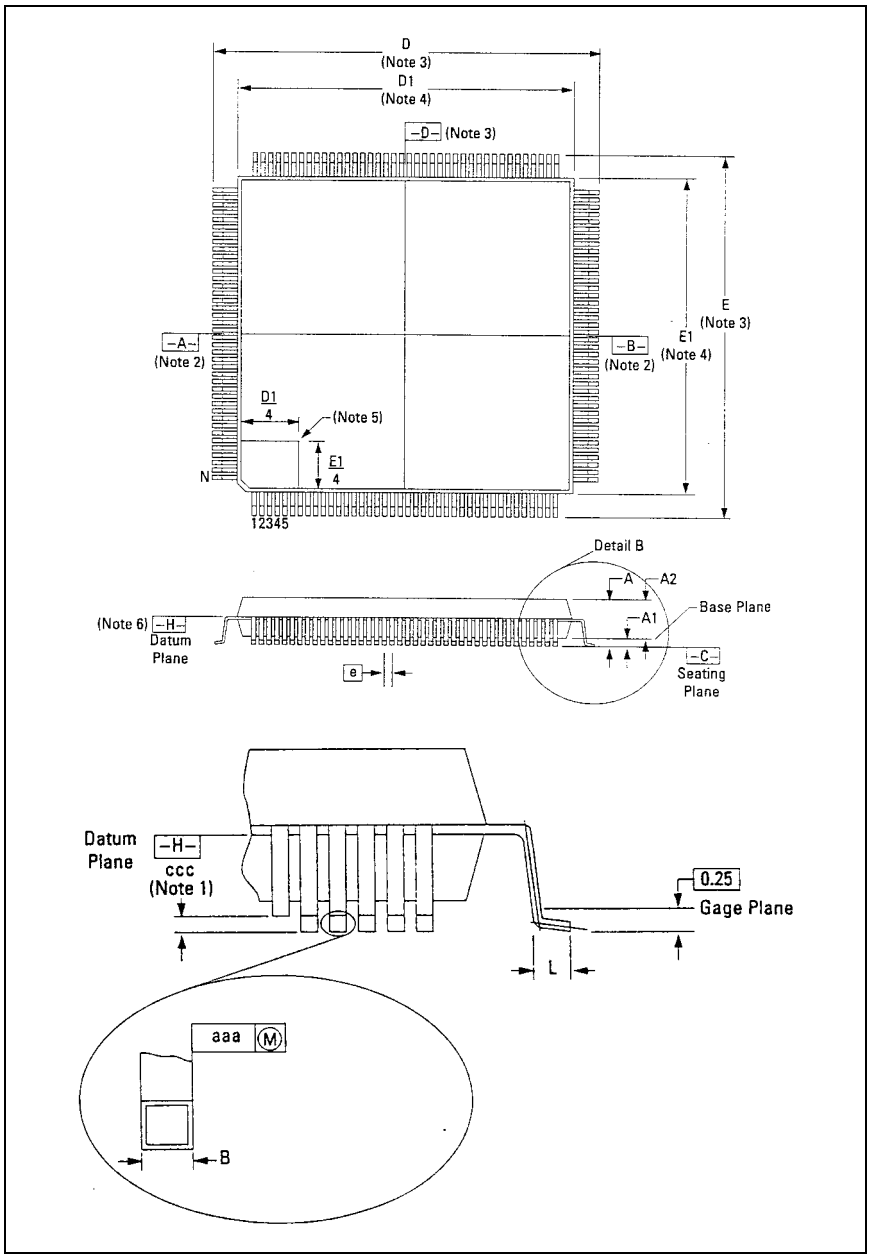

Figure 3. Dimension Diagram for the Alert on LAN ASIC

NOTES:

1. Coplanarity is the difference between the highest lead and the seating plane, -C-.
2. Datums A-B and -D- to be determined at Datum plane -H-.
3. Datum plane -D- To be determined at seating plane -C-.
4. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 millimeter/0.010 inch per side. Dimensions D1 and E1 do not include mold mismatch and are determined at Datum plane -H-.
5. Details of pin 1 identifier are optional but must be located within the zone indicated.

6. Datum plane -H- is located at the mold parting line and is coincident with the bottom of the leads where the lead exits the plastic body.
7. The drawing/dimensions are only for reference. For board layout, request a detailed engineering drawing from an LSI Logic sales office.

Table 5. Dimensions for the 44-pin TQFP Alert on LAN ASIC

Symbol	Min	Max	BSC
A	--	1.60	--
A1	0.05	--	--
A2	1.35	1.45	--
B	0.30	0.45	--
D	11.90	12.10	-
D1	9.90	10.10	--
e	--	--	0.80
E	11.90	12.10	--
E1	9.90	10.10	--
L	0.45	0.75	--
aaa	--	0.10	--
ccc	--	0.10	--

NOTE: All measurements are in millimeters.

8.0 Appendix A: Alert on LAN Supporting Hardware

The Alert on LAN ASIC is not a stand alone device. It requires additional components to create a functional management solution. One *possible* set of supporting hardware is identified in this appendix.

Note: Supporting hardware sets will differ from implementation to implementation.

- 82558 B-step device

  The 82558 Ethernet LAN Controller is required for a complete solution. The Alert on LAN ASIC is designed to communicate with the proprietary TCO interface of the 82558B. The 82558B provides the functionality to transmit data on the network and calculates and adds a 32-bit CRC to the data packet from the Alert on LAN ASIC.

- 64x16 1 MHz EEPROM

  The Alert on LAN ASIC is designed to use a 64x16 1 MHz EEPROM to configure the default settings upon reset and hard G2 transitions. If an EEPROM is not present or contains an invalid checksum, the Alert on LAN ASIC defaults to its component default settings as defined in section Section 4.0, “Configuration and Status Registers” on page 17.

  Note: The Alert on LAN ASIC requires the use of an EEPROM for its configuration settings; this is a separate EEPROM from the 82558B’s EEPROM.

- Environmental integrated circuit

  An environmental IC that is capable of monitoring voltage, temperature, and cover tamper can be used as part of the system management solution. However, only one input signal on the Alert on LAN ASIC exists (EVENT_2). If voltage is out of specification, the Alert on LAN ASIC expects to receive an event on the EVENT_2 signal. The Alert on LAN uses two other inputs, EVENT_3 (BTI Temperature) and EVENT_1 (Cover Tamper), to monitor these other events. This is required since the Alert on LAN ASIC does not have the ability to distinguish the difference between temperature and voltage events over one input signal.

- PIIX4 or equivalent

  The PCI-to-ISA/IDE Xcelerator (PIIX4) provides the SMB master interface that enables the system BIOS and OS to communicate with the Alert on LAN ASIC. PIIX4 also provides the PWR_GOOD and PCI_RST# signals that propagate to the Alert on LAN ASIC.

  Note: The PIIX4 has the ability to force the system into a low power state without prior indication to software. This is the reason the Alert on LAN ASIC monitors PWR_GOOD for a hard G2 transition.

- Sticky latch (optional)

  Sticky latches can are useful for detecting events that occur when the system is in a G3 state (completely off), such as Cover Tamper input. The latch can be battery-backed so that the Alert on LAN ASIC will become aware that an event occurred when it is powered-up. A sticky latch also provides the ability to be reset by driving the opposite polarity to the latch on the bidirectional pin, EVENT_1, of the Alert on LAN ASIC. The EVENT_1 pin of the Alert on LAN ASIC has the ability to clear a sticky latch. If this feature is enabled, it is executed by clearing the STA_EV1 bit in the Event Status register. The result is at least a 20 ms output

pulse of opposite polarity on the EVENT_1 pin. An example sticky latch circuit is illustrated in Figure 4.

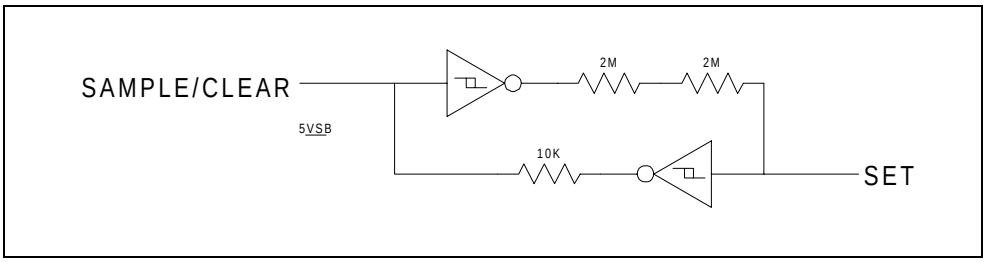

Figure 4. Sticky Latch Example

Note: This solution also prohibits the use of the ASIC cover tamper clear mechanism (the ASIC can be configured to output a 20 ms clear pulse). The environmental IC should clear the sticky latch.